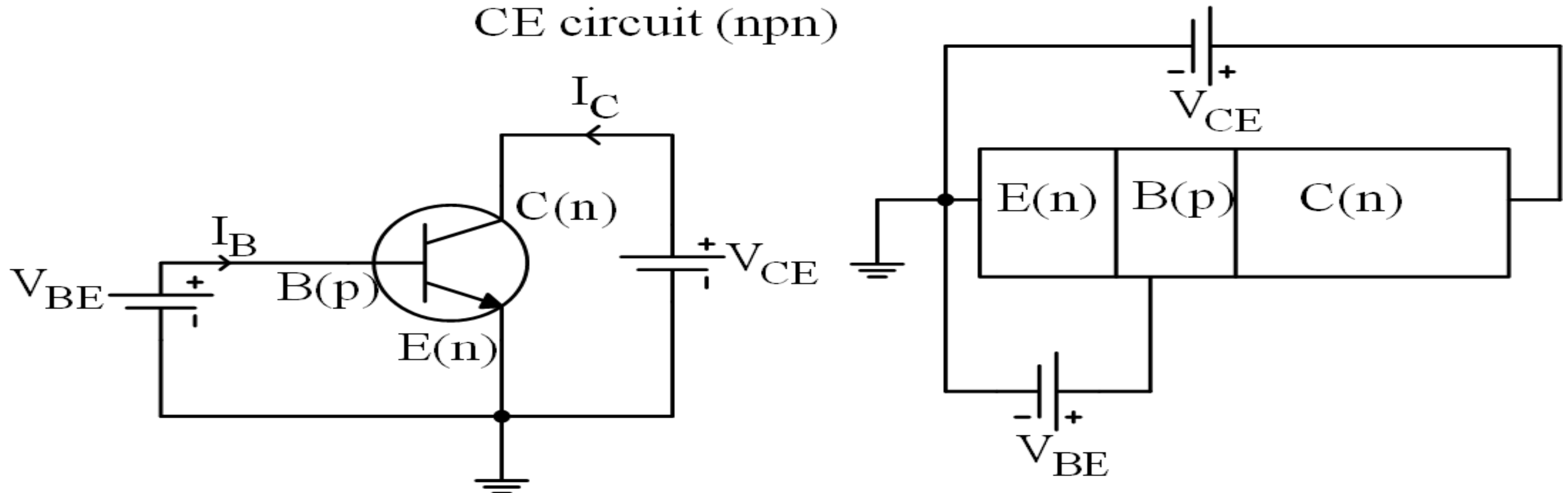
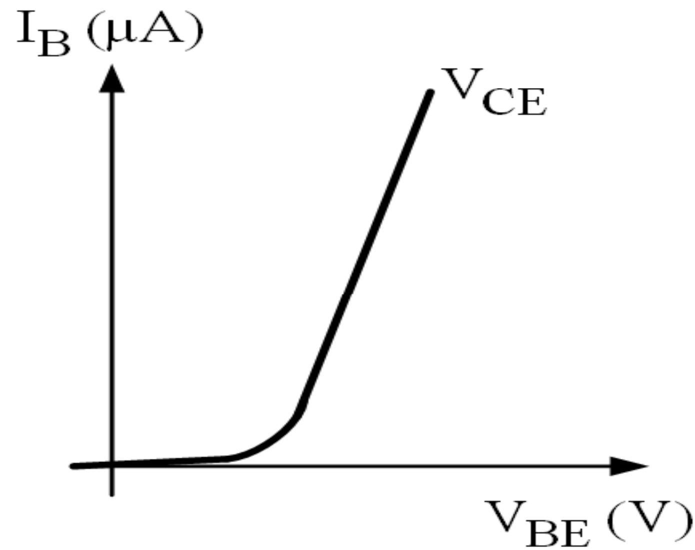
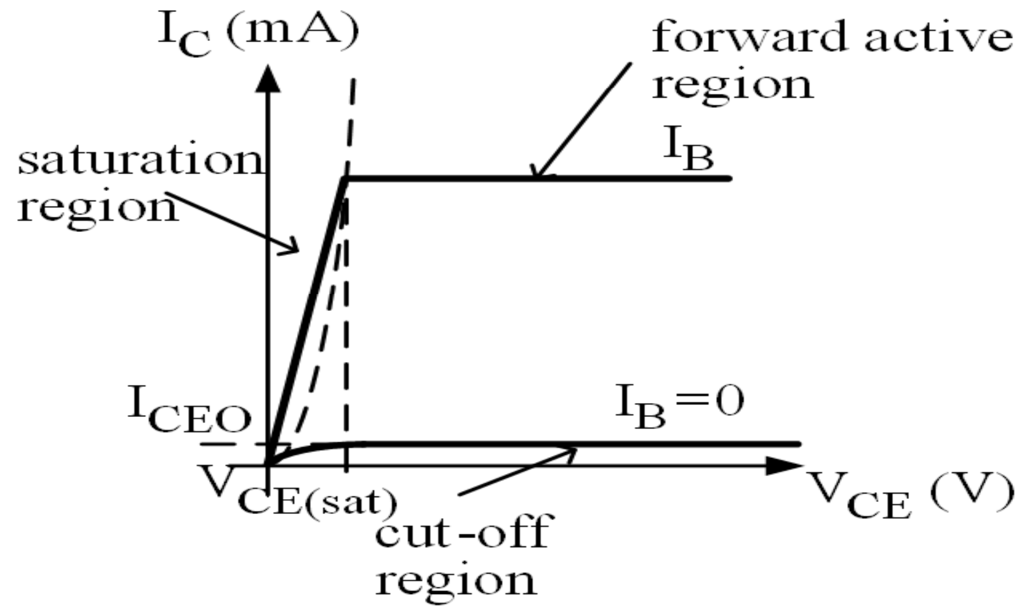
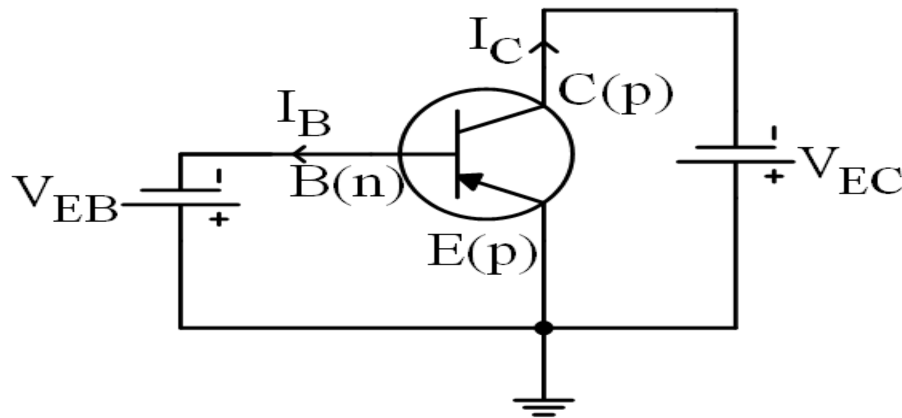
CLASS 6&7

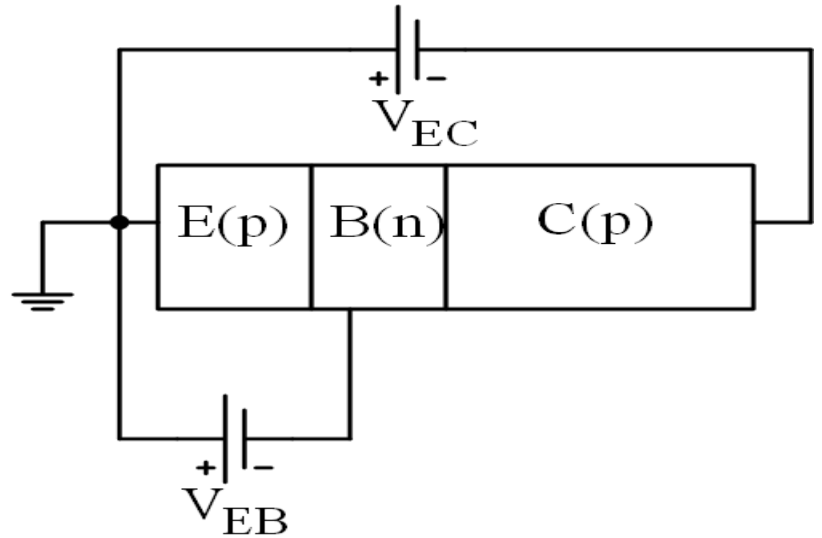
BJT PARAMETERS AND BIASING


CE circuit (npn)
I_C
C(n)
I_B
V_BE
B(p)
E(n)
V_CE
E(n)
B(p)
C(n)
V_CE
V_BE
forward active region: |V_CE|>|V_BE|

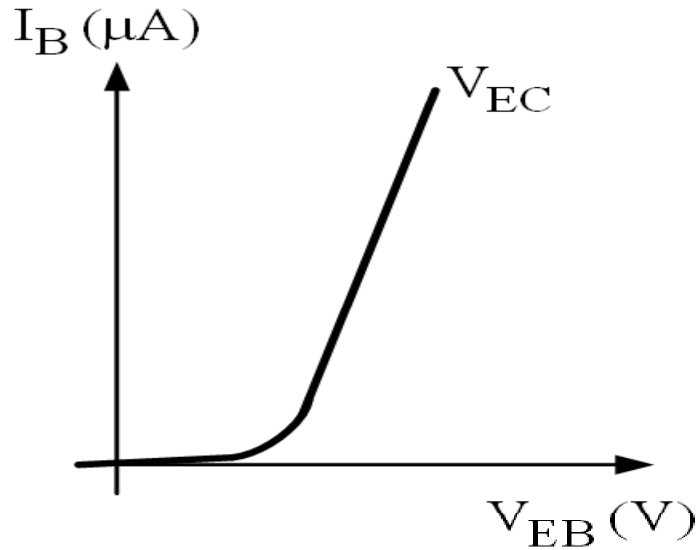

input characteristic
I_B (μA)
V_CE
V_BE (V)

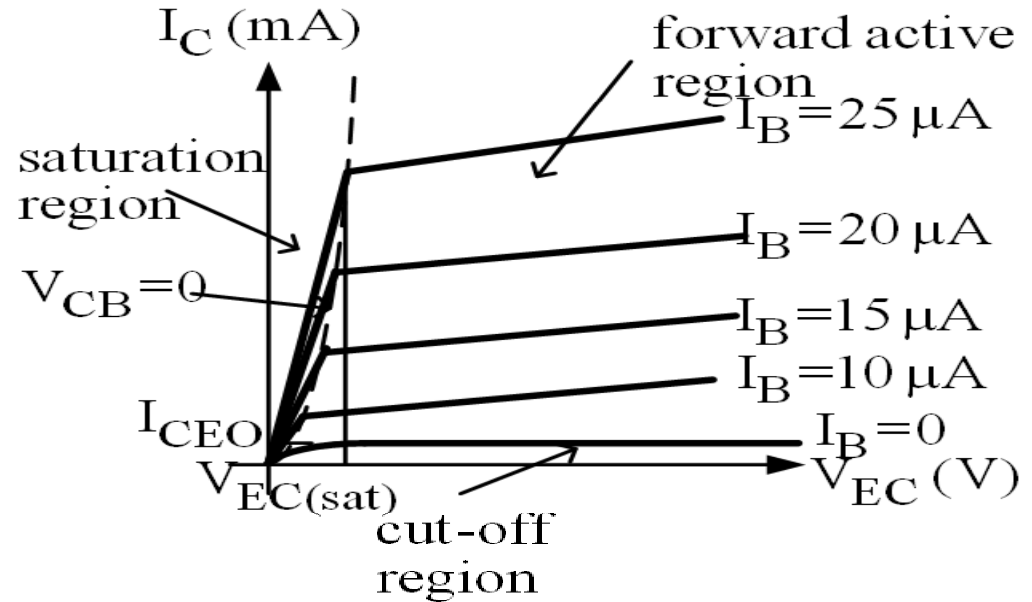

output characteristic
I_C (mA)
forward active region
saturation region
I_B
I_CEO
I_B =0
V_CE(sat)
cut-off region
V_CE (V)





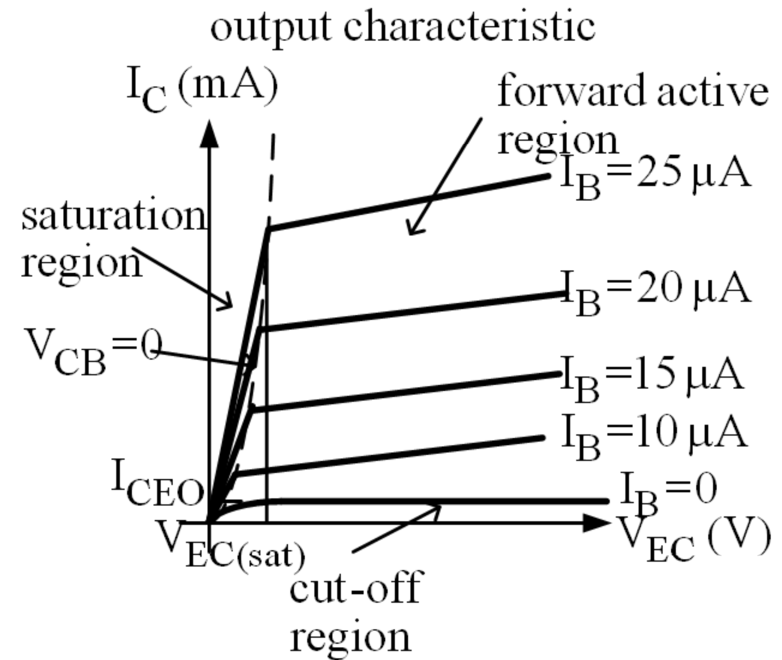
forward active region: $|V_{EC}| > |V_{EB}|$

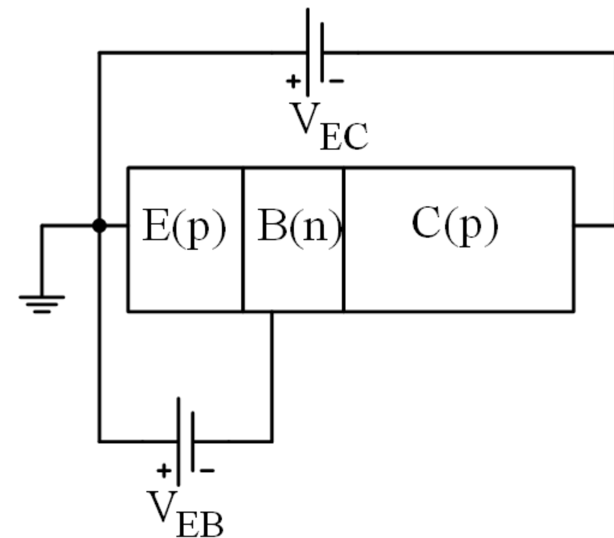




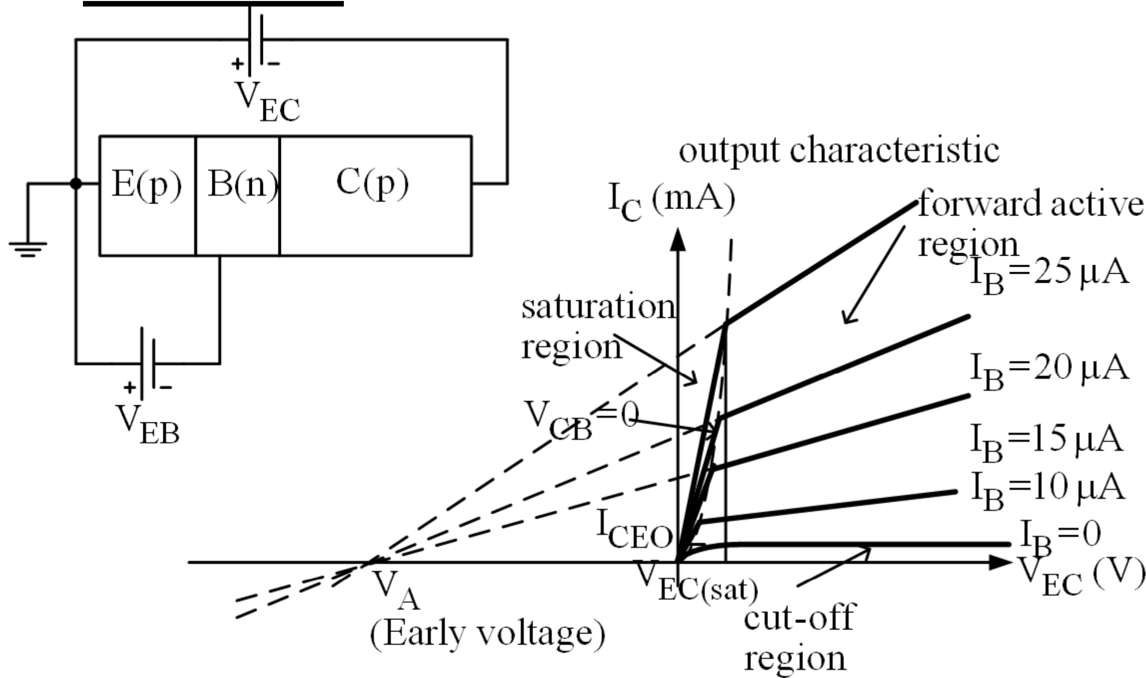
Observations:

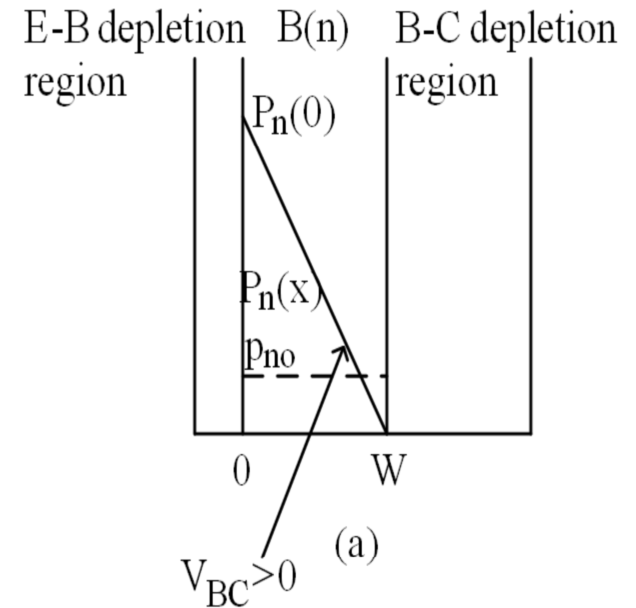
- **For an ideal transistor in the CE configuration, I_C for a fixed I_B is independent of V_{EC} for $V_{EC}>V_{EC(sat)}$. This condition is true if the effective width of the B is fixed.**
- **As the width of the depletion region in B of the B-C junction is dependent on V_{EC} , the effective width of B will also be dependent on V_{EC}. Therefore, I_C will be dependent on V_{EC} although $V_{EC}>V_{EC(sat)}$. For a fixed I_B and $V_{EC}>V_{EC(sat)}$, I_C ↑ when V_{EC} ↑. However, the increment is small when compared to the increment of I_C with the increase in V_{EC} when the transistor is in the saturation region.**

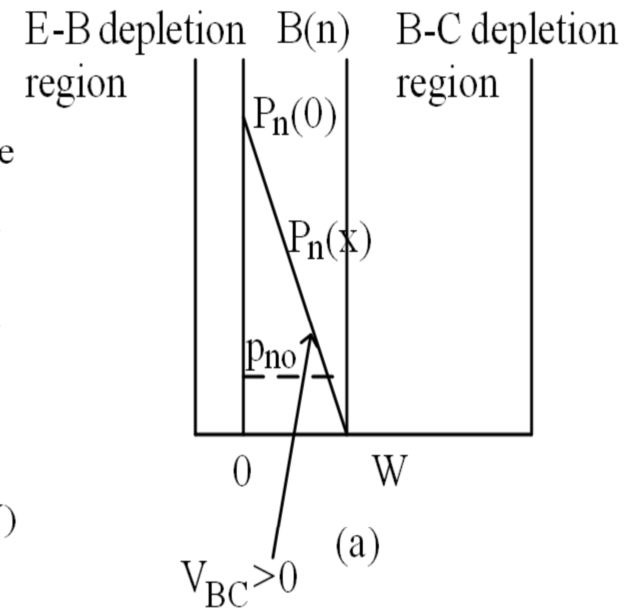


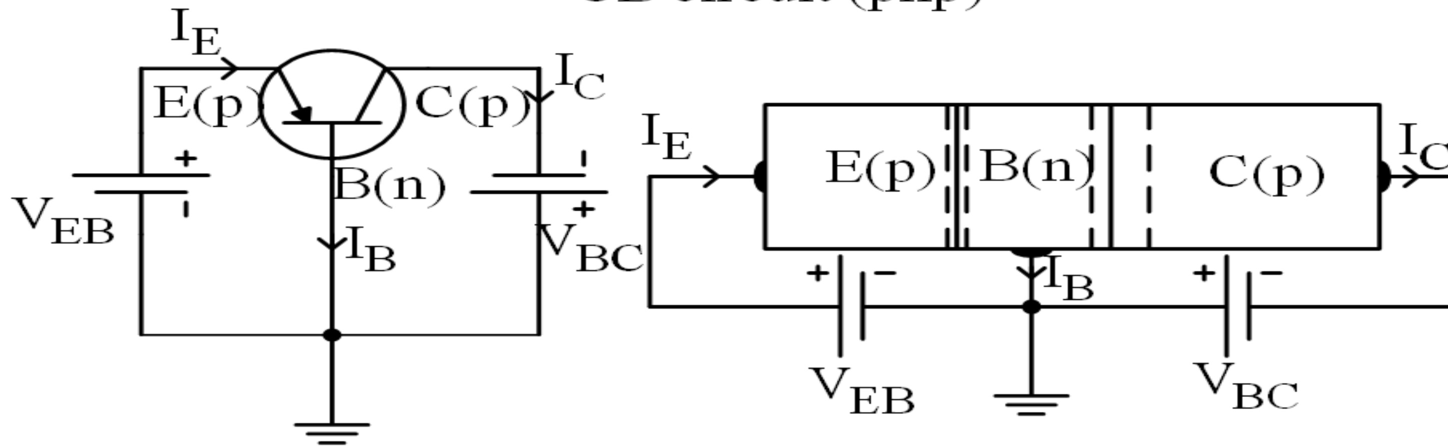


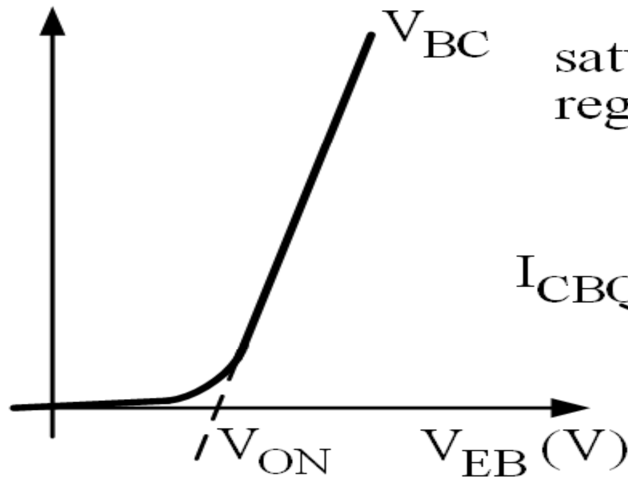
- **When V_{EC} ↑, B-C junction becomes more rb, depletion region of B-C junction ↑ , effective width of B ↓. Less recombination happen in B (or the slope of the hole density in B ↑), and therefore I_C ↑.**
- **The phenomena where I_C ↑ when V_{EC} ↑ is called the <u>Early effect</u> or <u>base width modulation</u>.**

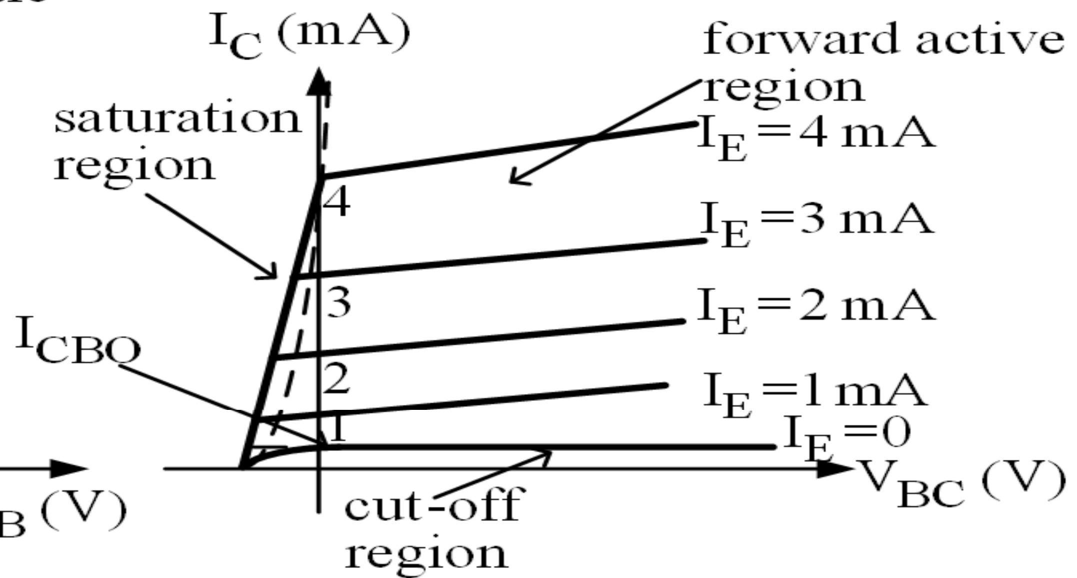










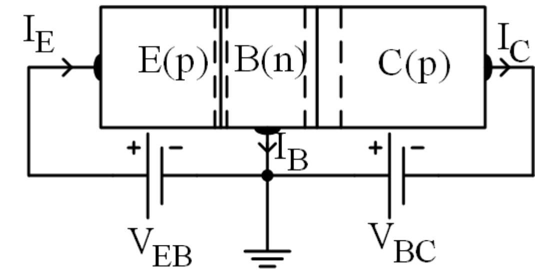


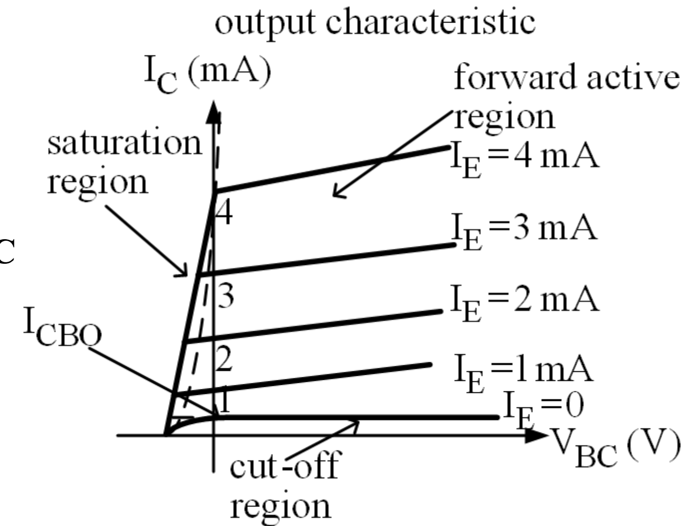
In the active region, $I_C \approx I_E$ and is independent of V_{BC}. $I_C \approx \alpha_o I_E$

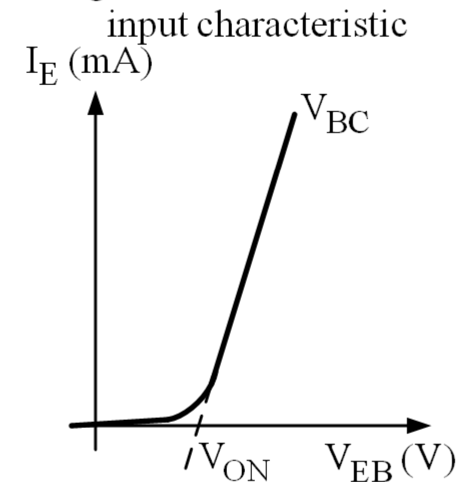
α_o is the CB current gain.

<u>**Observations**</u>

- **V_{BC}↑ I_C↑ because when V_{BC}↑, the B-C junction becomes more rb. The width of the effective B region (outside depletion) becomes smaller. Recombinations ↓. Hence, I_C↑.**
- **At a fixed V_{BC} , if I_E↑ I_C↑. This is because, I_E↑ when V_{EB}↑. As $I_C = \alpha_o I_E$ and $\alpha_o \approx 1$, $I_C \approx I_E$. Thus, I_E↑ I_C↑.**
- **If $V_{BC} = 0$, there still exists a depletion region at the B-C junction. Fixed –ve ions in the depletion region of the C can still manage to attract the holes from B to cross the B-C junction and enter C. I_C exists. If the V_{BC} becomes –ve (i.e. V_C is more +ve than V_B), the width of the depletion region↓ and I_C ↓. When $V_{CB} \approx V_{ON}$, the depletion region's width ≈ 0. At this time, the B-C junction becomes fb and $I_C = 0$.**



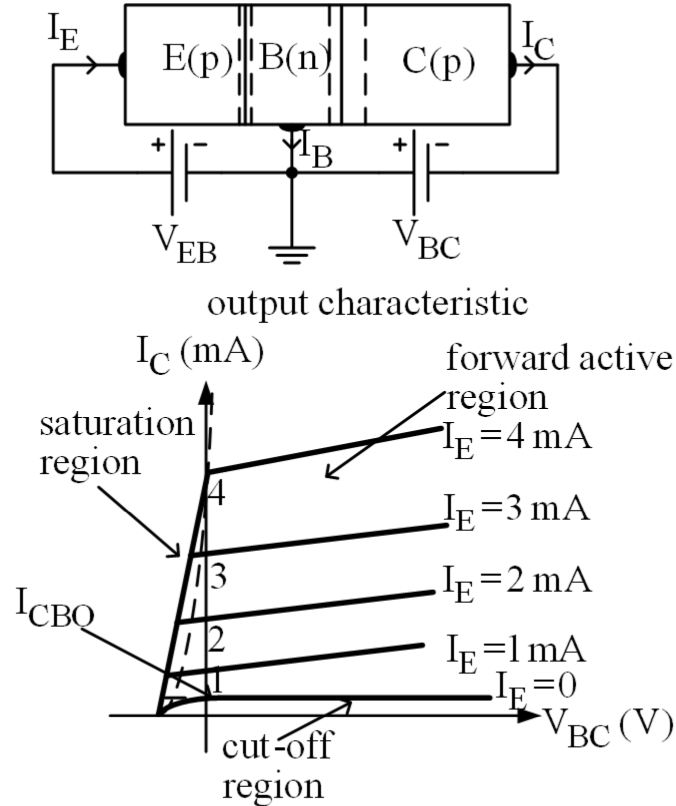


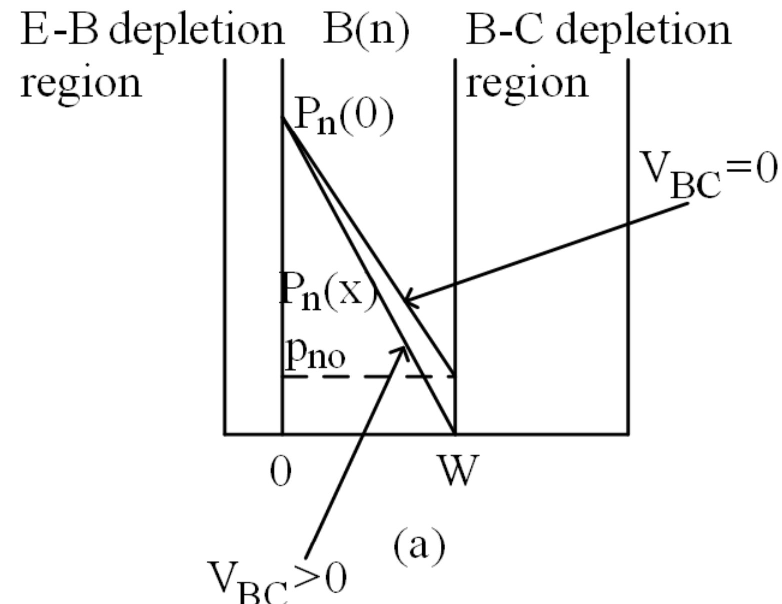


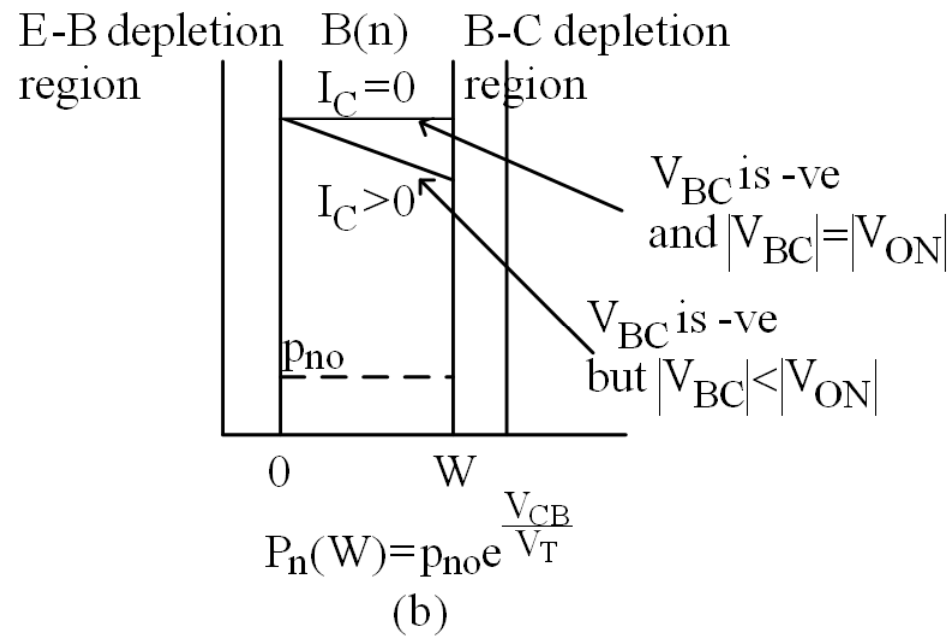
Distribution of minority carriers in B for a pnp transistor.

(a) Active mode for $|V_{BC}| \geq 0$.

(b) Saturation mode with both E-B and B-C junctions fb.



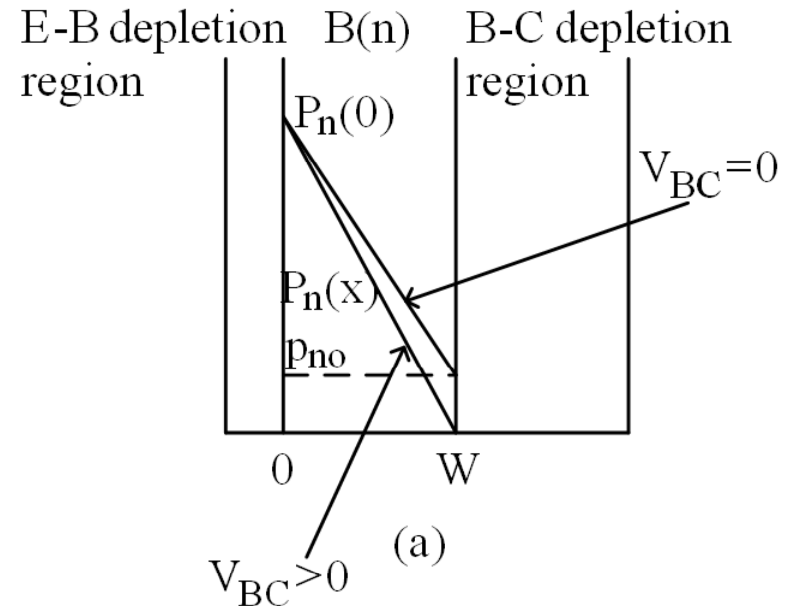


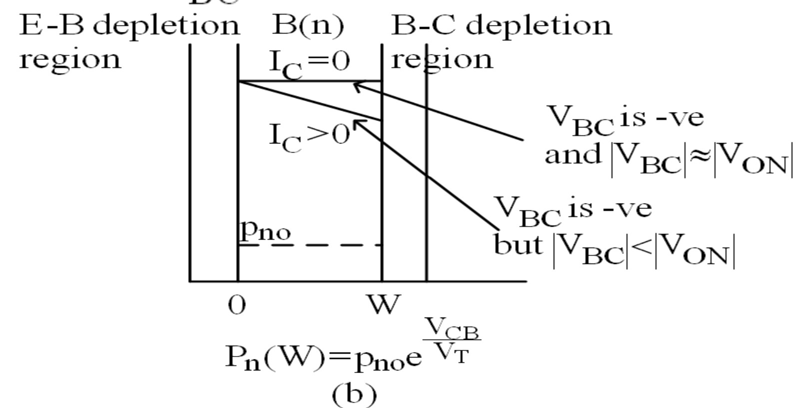


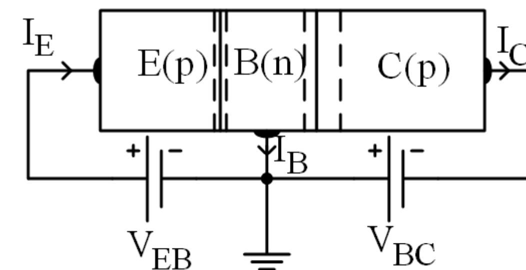
Observations

- **Since the difference in the slope is not large when $V_{BC} > 0$ and $V_{BC} = 0$, I_C does not change much.**
- **$I_C = 0$ when one small forward voltage is supplied across the B-C junction ($V_{BC} \approx -1$ V for Silicon). Under this condition, the transistor is in the saturation region.**
- **The fb supplied to the B-C junction will increase the hole density at x=W until it reaches a value equals to the hole density at x=0. This means that the hole gradient is 0 and consequently I_C will reduce to 0.**

$$I_{Cp} = A\left[-qD_p \frac{dp_n}{dx}\bigg|_{x=W}\right] \approx \frac{qAD_p p_{no}}{W} e^{(qV_{EB})/kT}, \quad I_{Cn} = A\left[qD_C \frac{dn_C}{dx}\bigg|_{x=x_C}\right] = \frac{qAD_C n_{Co}}{L_C}$$







Important observations:

$I_E = I_B + I_C$

For the CB,

$I_C = \alpha_o I_E + I_{CBO}$

where I_{CBO} is the C-B current when E is open ($I_E = 0$) and it is a minority carrier current.

$I_C = \alpha_o (I_B + I_C) + I_{CBO}$

$I_C (1 - \alpha_o) = \alpha_o I_B + I_{CBO}$

$I_C = (\alpha_o I_B + I_{CBO}) / (1 - \alpha_o) = [\alpha_o I_B / (1 - \alpha_o)] + [I_{CBO} / (1 - \alpha_o)]$

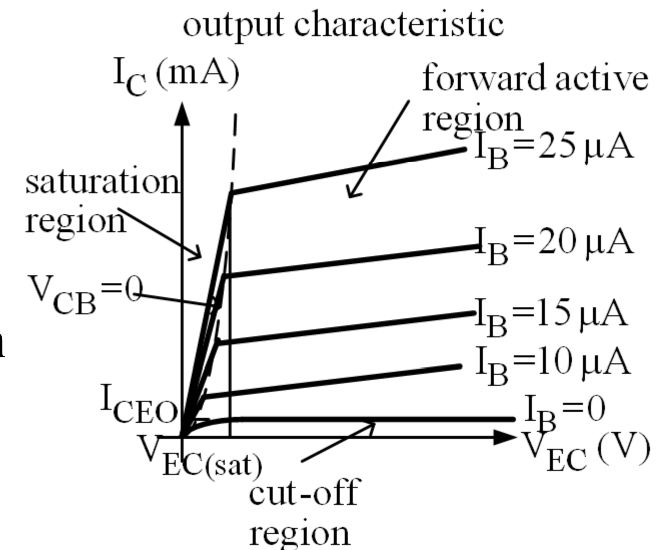
$\alpha_o / (1 - \alpha_o) = \beta_{DC}$ = CE DC current gain

$\beta_{DC} = \Delta I_C / \Delta I_B$

$I_{CEO} = I_{CBO} / (1 - \alpha_o)$

where I_{CEO} is the leakage current when B is open ($I_B = 0$) and it is a minority carrier current.

$I_C = \beta_{DC} I_B + I_{CEO}$



$\alpha_o / (1 - \alpha_o) = \beta_{DC}$

$\alpha_o = \beta_{DC} (1 - \alpha_o)$

$\alpha_o + \beta_{DC} \alpha_o = \beta_{DC}$

$\alpha_o (1 + \beta_{DC}) = \beta_{DC}$

$\alpha_o = \beta_{DC} / (1 + \beta_{DC})$

β_{DC} = α_o / (1 – α_o); this expression shows that β_{DC}>1

$\alpha_o = \beta_{DC} /(1 + \beta_{DC})$; this expression shows that α_o< 1

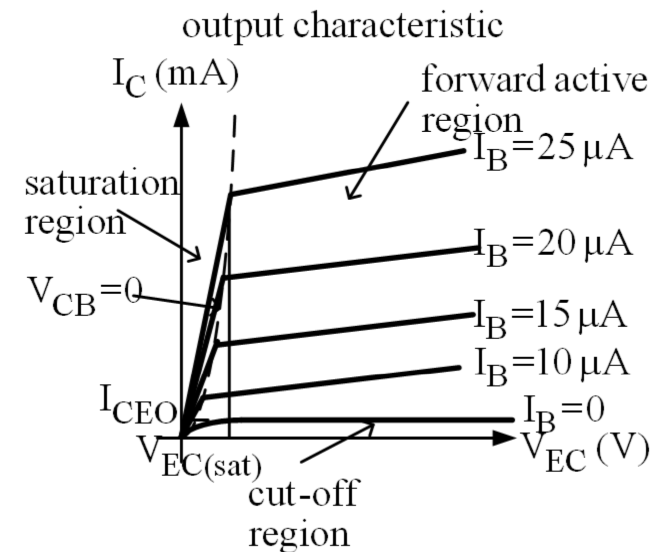
$\alpha_o \approx 1$. Thus, $\beta_{DC} >> 1$.

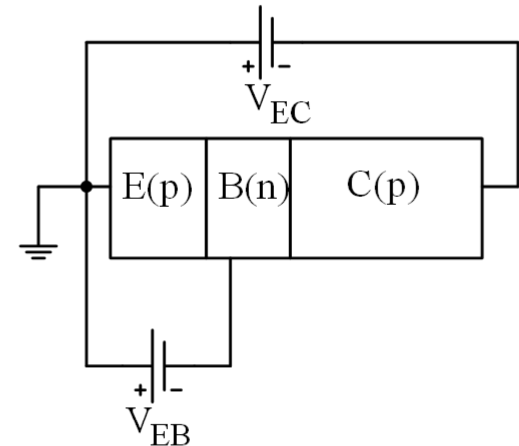
If α_o = 0.99, β_{DC} = 0.99 / (1 – 0.99) = 99.

If α_o = 0.998, β_{DC} = 0.998 / (1 – 0.998) = 499.

These results show that a small change in I_B will cause a large difference in I_C .

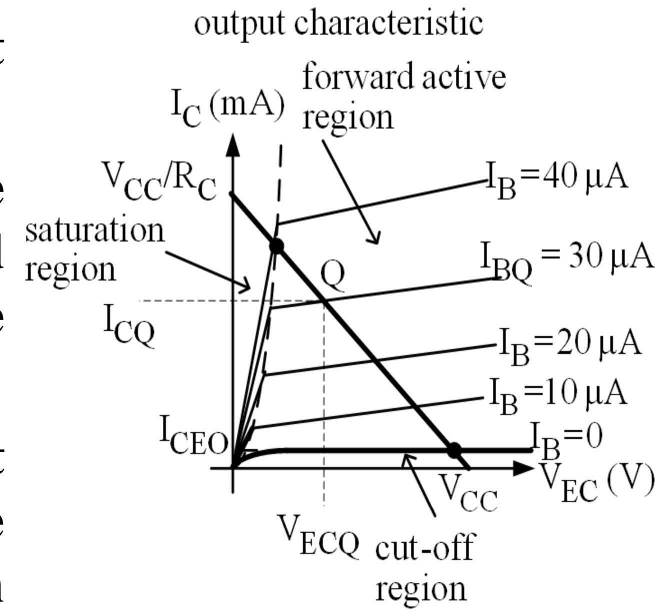
From the output characteristics of the CE, there is still output current, I_C, flowing although I_B = 0 and this is the I_{CEO} which is the leakage current when I_B=0.



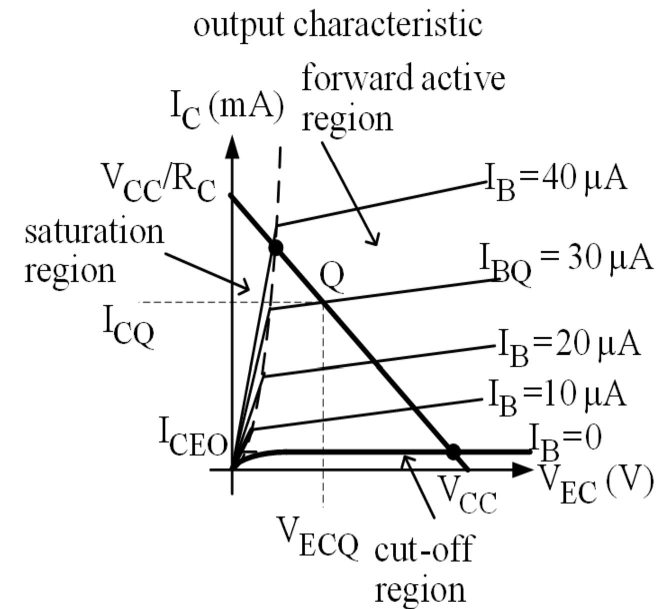


BIASING

- The BJT must be biased in order to operate it as an amplifier.
- A DC operating point must be set so that the signal at the input terminal can be amplified and reproduced without any distortion at the output terminal.
- For the CE amplifier, the DC operating point is I_C and V_{CE} (for npn or V_{EC} for pnp). The operating point must be in the active region in order for the BJT to operate as an amplifier.
- The DC operating point is known as the quiescent (Q) point. For the CE amplifier, the Q point is I_{CQ} and V_{CEQ}.
- With the correct biasing, the circuit need not be changed or redesign when another transistor from the same type is substituted or when the temperature changes. In other words, a biasing circuit needs to be stable.



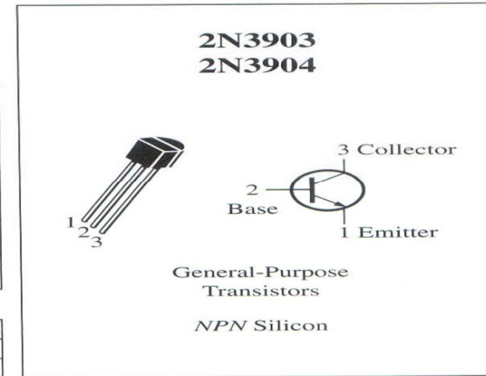
To determine the operating point:



- **The DC load line is drawn on the output characteristic to determine the operating current and voltage of the circuit. The intersection of the load line with the I and V axis depends on the circuit's schematic.**

- **A DC biasing point / quiescent (Q) point is determined from the load line in the active region. The Q point is a point on the load line that represents the current and voltage at the output of a transistor when there is no AC signal. The stability of a biasing point is influenced by the change in the parameters (as an example: β_{DC}) when the transistor is replaced by another transistor of the same type or by the change in temperature.**

From Floyd, Electronic Devices, Sixth Edition.



Maximum Ratings

Rating	Symbol	Value	Unit
Collector-Emitter voltage	V_{CEO}	40	V dc
Collector-Base voltage	V_{CBO}	60	V dc
Emitter-Base voltage	V_{EBO}	6.0	V dc
Collector current — continuous	I_C	200	mA dc
Total device dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	625 5.0	mW mW/°C
Total device dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and storage junction Temperature range	T_J, T_{stg}	−55 to +150	°C

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal resistance, junction to case	$R_{\theta JC}$	83.3	°C/W
Thermal resistance, junction to ambient	$R_{\theta JA}$	200	°C/W

Electrical Characteristics ($T_A = 25°C$ unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF Characteristics					
Collector-Emitter breakdown voltage ($I_C = 1.0$ mA dc, $I_B = 0$)		$V_{(BR)CEO}$	40	–	V dc
Collector-Base breakdown voltage ($I_C = 10$ µA dc, $I_E = 0$)		$V_{(BR)CBO}$	60	–	V dc
Emitter-Base breakdown voltage ($I_E = 10$ µA dc, $I_C = 0$)		$V_{(BR)EBO}$	6.0	–	V dc
Base cutoff current ($V_{CE} = 30$ V dc, $V_{EB} = 3.0$ V dc)		I_{BL}	–	50	nA dc
Collector cutoff current ($V_{CE} = 30$ V dc, $V_{EB} = 3.0$ V dc)		I_{CEX}	–	50	nA dc
ON Characteristics					
DC current gain ($I_C = 0.1$ mA dc, $V_{CE} = 1.0$ V dc)	2N3903 2N3904	h_{FE}	20 40	– –	–
($I_C = 1.0$ mA dc, $V_{CE} = 1.0$ V dc)	2N3903 2N3904		35 70	– –	
($I_C = 10$ mA dc, $V_{CE} = 1.0$ V dc)	2N3903 2N3904		50 100	150 300	
($I_C = 50$ mA dc, $V_{CE} = 1.0$ V dc)	2N3903 2N3904		30 60	– –	
($I_C = 100$ mA dc, $V_{CE} = 1.0$ V dc)	2N3903 2N3904		15 30	– –	
Collector-Emitter saturation voltage ($I_C = 10$ mA dc, $I_B = 1.0$ mA dc) ($I_C = 50$ mA dc, $I_B = 5.0$ mA dc)		$V_{CE(sat)}$	– –	0.2 0.3	V dc
Base-Emitter saturation voltage ($I_C = 10$ mA dc, $I_B = 1.0$ mA dc) ($I_C = 50$ mA dc, $I_B = 5.0$ mA dc)		$V_{BE(sat)}$	0.65 –	0.85 0.95	V dc

▲ **FIGURE 4–19**

Partial transistor data sheet.